

Contents

CHAPTER	Introduction	1
1	1.1 Overview	1
	1.2 The Main Components of a Computer	3
	1.3 An Example System: Wading through the Jargon	4
	1.4 Standards Organizations	15
	1.5 Historical Development	16
	1.5.1 Generation Zero: Mechanical Calculating Machines (1642–1945)	17
	1.5.2 The First Generation: Vacuum Tube Computers (1945–1953)	19
	1.5.3 The Second Generation: Transistorized Computers (1954–1965)	23
	1.5.4 The Third Generation: Integrated Circuit Computers (1965–1980)	26
	1.5.5 The Fourth Generation: VLSI Computers (1980–????)	26
	1.5.6 Moore’s Law	30
	1.6 The Computer Level Hierarchy	31
	1.7 The von Neumann Model	34
	1.8 Non-von Neumann Models	37
	Chapter Summary	40
	Further Reading	41
	References	42
	Review of Essential Terms and Concepts	43
	Exercises	44

CHAPTER	Data Representation in Computer Systems	47
2	2.1 Introduction	47
	2.2 Positional Numbering Systems	48

vi Contents

2.3	Converting Between Bases	48
2.3.1	Converting Unsigned Whole Numbers	49
2.3.2	Converting Fractions	51
2.3.3	Converting between Power-of-Two Radices	54
2.4	Signed Integer Representation	54
2.4.1	Signed Magnitude	54
2.4.2	Complement Systems	60
2.4.3	Unsigned Versus Signed Numbers	66
2.4.4	Computers, Arithmetic, and Booth's Algorithm	66
2.4.5	Carry Versus Overflow	70
2.4.6	Binary Multiplication and Division Using Shifting	71
2.5	Floating-Point Representation	73
2.5.1	A Simple Model	74
2.5.2	Floating-Point Arithmetic	76
2.5.3	Floating-Point Errors	78
2.5.4	The IEEE-754 Floating-Point Standard	79
2.5.5	Range, Precision, and Accuracy	81
2.5.6	Additional Problems with Floating-Point Numbers	82
2.6	Character Codes	85
2.6.1	Binary-Coded Decimal	86
2.6.2	EBCDIC	87
2.6.3	ASCII	88
2.6.4	Unicode	88
2.7	Error Detection and Correction	92
2.7.1	Cyclic Redundancy Check	92
2.7.2	Hamming Codes	95
2.7.3	Reed-Solomon	102
	Chapter Summary	103
	Further Reading	103
	References	104
	Review of Essential Terms and Concepts	105
	Exercises	106
	Focus on Codes for Data Recording and Transmission	113
2A.1	Non-Return-to-Zero Code	113
2A.2	Non-Return-to-Zero-Invert Code	114
2A.3	Phase Modulation (Manchester Code)	115
2A.4	Frequency Modulation	116
2A.5	Run-Length-Limited Code	116
2A.6	Partial Response Maximum Likelihood Coding	119
2A.7	Summary	120
	Exercises	120

CHAPTER	Boolean Algebra and Digital Logic	121
3		
3.1	Introduction 121	
3.2	Boolean Algebra 122	
3.2.1	Boolean Expressions 123	
3.2.2	Boolean Identities 124	
3.2.3	Simplification of Boolean Expressions 126	
3.2.4	Complements 128	
3.2.5	Representing Boolean Functions 130	
3.3	Logic Gates 131	
3.3.1	Symbols for Logic Gates 132	
3.3.2	Universal Gates 132	
3.3.3	Multiple Input Gates 133	
3.4	Digital Components 134	
3.4.1	Digital Circuits and Their Relationship to Boolean Algebra 134	
3.4.2	Integrated Circuits 136	
3.5	Combinational Circuits 138	
3.5.1	Basic Concepts 138	
3.5.2	Examples of Typical Combinational Circuits 138	
3.6	Sequential Circuits 145	
3.6.1	Basic Concepts 146	
3.6.2	Clocks 146	
3.6.3	Flip-Flops 146	
3.6.4	Finite State Machines 150	
3.6.5	Examples of Sequential Circuits 155	
3.6.6	An Application of Sequential Logic: Convolutional Coding and Viterbi Detection 160	
3.7	Designing Circuits 166	
	Chapter Summary 167	
	Further Reading 167	
	References 169	
	Review of Essential Terms and Concepts 169	
	Exercises 170	
	Focus on Karnaugh Maps 181	
3A.1	Introduction 181	
3A.2	Description of Kmaps and Terminology 181	
3A.3	Kmap Simplification for Two Variables 183	
3A.4	Kmap Simplification for Three Variables 185	
3A.5	Kmap Simplification for Four Variables 187	

viii Contents

- 3A.6 Don't Care Conditions 190
- 3A.7 Summary 191
- Exercises 192

CHAPTER	MARIE: An Introduction to a Simple Computer	195
4		
4.1	Introduction 195	
4.2	CPU Basics and Organization 195	
4.2.1	The Registers 196	
4.2.2	The ALU 197	
4.2.3	The Control Unit 197	
4.3	The Bus 197	
4.4	Clocks 201	
4.5	The Input/Output Subsystem 203	
4.6	Memory Organization and Addressing 204	
4.7	Interrupts 208	
4.8	MARIE 209	
4.8.1	The Architecture 209	
4.8.2	Registers and Buses 211	
4.8.3	Instruction Set Architecture 212	
4.8.4	Register Transfer Notation 215	
4.9	Instruction Processing 218	
4.9.1	The Fetch-Decode-Execute Cycle 218	
4.9.2	Interrupts and the Instruction Cycle 219	
4.9.3	MARIE's I/O 223	
4.10	A Simple Program 223	
4.11	A Discussion on Assemblers 226	
4.11.1	What Do Assemblers Do? 226	
4.11.2	Why Use Assembly Language? 228	
4.12	Extending Our Instruction Set 229	
4.13	A Discussion on Decoding: Hardwired Versus Microprogrammed Control 235	
4.13.1	Machine Control 235	
4.13.2	Hardwired Control 238	
4.13.3	Microprogrammed Control 242	
4.14	Real-World Examples of Computer Architectures 246	
4.14.1	Intel Architectures 247	

4.14.2	MIPS Architectures	253
	Chapter Summary	255
	Further Reading	257
	References	257
	Review of Essential Terms and Concepts	259
	Exercises	260

CHAPTER 5

A Closer Look at Instruction Set Architectures 269

5.1	Introduction	269
5.2	Instruction Formats	269
5.2.1	Design Decisions for Instruction Sets	270
5.2.2	Little Versus Big Endian	271
5.2.3	Internal Storage in the CPU: Stacks Versus Registers	273
5.2.4	Number of Operands and Instruction Length	274
5.2.5	Expanding Opcodes	280
5.3	Instruction Types	285
5.3.1	Data Movement	285
5.3.2	Arithmetic Operations	285
5.3.3	Boolean Logic Instructions	285
5.3.4	Bit Manipulation Instructions	286
5.3.5	Input/Output Instructions	286
5.3.6	Instructions for Transfer of Control	287
5.3.7	Special Purpose Instructions	287
5.3.8	Instruction Set Orthogonality	287
5.4	Addressing	288
5.4.1	Data Types	288
5.4.2	Address Modes	288
5.5	Instruction Pipelining	291
5.6	Real-World Examples of ISAs	297
5.6.1	Intel	297
5.6.2	MIPS	298
5.6.3	Java Virtual Machine	298
	Chapter Summary	302
	Further Reading	303
	References	304
	Review of Essential Terms and Concepts	305
	Exercises	306

CHAPTER	Memory	313
6		
6.1	Introduction 313	
6.2	Types of Memory 313	
6.3	The Memory Hierarchy 315	
6.3.1	Locality of Reference 318	
6.4	Cache Memory 319	
6.4.1	Cache Mapping Schemes 321	
6.4.2	Replacement Policies 333	
6.4.3	Effective Access Time and Hit Ratio 334	
6.4.4	When Does Caching Break Down? 335	
6.4.5	Cache Write Policies 335	
6.4.6	Instruction and Data Caches 338	
6.4.7	Levels of Cache 339	
6.5	Virtual Memory 340	
6.5.1	Paging 341	
6.5.2	Effective Access Time Using Paging 349	
6.5.3	Putting It All Together: Using Cache, TLBs, and Paging 350	
6.5.4	Advantages and Disadvantages of Paging and Virtual Memory 352	
6.5.5	Segmentation 353	
6.5.6	Paging Combined with Segmentation 354	
6.6	A Real-World Example of Memory Management 355	
	Chapter Summary 356	
	Further Reading 357	
	References 357	
	Review of Essential Terms and Concepts 358	
	Exercises 359	

CHAPTER	Input/Output and Storage Systems	367
7		
7.1	Introduction 367	
7.2	I/O and Performance 368	
7.3	Amdahl's Law 368	
7.4	I/O Architectures 372	
7.4.1	I/O Control Methods 373	
7.4.2	Character I/O Versus Block I/O 381	
7.4.3	I/O Bus Operation 382	

7.5	Data Transmission Modes	385
7.5.1	Parallel Data Transmission	386
7.5.2	Serial Data Transmission	389
7.6	Magnetic Disk Technology	389
7.6.1	Rigid Disk Drives	391
7.6.2	Solid State Disks	395
7.7	Optical Disks	396
7.7.1	CD-ROM	396
7.7.2	DVD	400
7.7.3	Blue-Violet Laser Disks	401
7.7.4	Optical Disk Recording Methods	402
7.8	Magnetic Tape	403
7.9	RAID	407
7.9.1	RAID Level 0	408
7.9.2	RAID Level 1	409
7.9.3	RAID Level 2	409
7.9.4	RAID Level 3	410
7.9.5	RAID Level 4	411
7.9.6	RAID Level 5	412
7.9.7	RAID Level 6	413
7.9.8	RAID DP	414
7.9.9	Hybrid RAID Systems	416
7.10	The Future of Data Storage	416
	Chapter Summary	420
	Further Reading	420
	References	421
	Review of Essential Terms and Concepts	422
	Exercises	424
	Focus on Data Compression	429
7A.1	Introduction	429
7A.2	Statistical Coding	431
7A.2.1	Huffman Coding	432
7A.2.2	Arithmetic Coding	436
7A.3	Ziv-Lempel (LZ) Dictionary Systems	439
7A.4	GIF and PNG Compression	443
7A.5	JPEG Compression	444
7A.6	Summary	448
	Exercises	449

CHAPTER	System Software	451
8	8.1 Introduction 451	
	8.2 Operating Systems 452	
	8.2.1 Operating Systems History 453	
	8.2.2 Operating System Design 458	
	8.2.3 Operating System Services 460	
	8.3 Protected Environments 464	
	8.3.1 Virtual Machines 465	
	8.3.2 Subsystems and Partitions 468	
	8.3.3 Protected Environments and the Evolution of Systems Architectures 470	
	8.4 Programming Tools 472	
	8.4.1 Assemblers and Assembly 472	
	8.4.2 Link Editors 475	
	8.4.3 Dynamic Link Libraries 476	
	8.4.4 Compilers 478	
	8.4.5 Interpreters 482	
	8.5 Java: All of the Above 483	
	8.6 Database Software 489	
	8.7 Transaction Managers 495	
	Chapter Summary 497	
	Further Reading 499	
	References 500	
	Review of Essential Terms and Concepts 500	
	Exercises 501	

CHAPTER	Alternative Architectures	505
9	9.1 Introduction 505	
	9.2 RISC Machines 506	
	9.3 Flynn's Taxonomy 511	
	9.4 Parallel and Multiprocessor Architectures 515	
	9.4.1 Superscalar and VLIW 516	
	9.4.2 Vector Processors 518	
	9.4.3 Interconnection Networks 519	
	9.4.4 Shared Memory Multiprocessors 524	
	9.4.5 Distributed Computing 528	

9.5 Alternative Parallel Processing Approaches 531

9.5.1 Dataflow Computing 531

9.5.2 Neural Networks 534

9.5.3 Systolic Arrays 537

9.6 Quantum Computing 539

Chapter Summary 541

Further Reading 542

References 542

Review of Essential Terms and Concepts 544

Exercises 545

**CHAPTER
10****Topics in Embedded Systems****549****10.1 Introduction 549****10.2 An Overview of Embedded Hardware 551**

10.2.1 Off-the-Shelf Embedded System Hardware 551

10.2.2 Configurable Hardware 555

10.2.3 Custom-Designed Embedded Hardware 562

10.3 An Overview of Embedded Software 570

10.3.1 Embedded Systems Memory Organization 571

10.3.2 Embedded Operating Systems 572

10.3.3 Embedded Systems Software Development 575

Chapter Summary 577

Further Reading 579

References 580

Review of Essential Terms and Concepts 581

Exercises 582

**CHAPTER
11****Performance Measurement and Analysis****585****11.1 Introduction 585****11.2 Computer Performance Equations 586****11.3 Mathematical Preliminaries 587**

11.3.1 What the Means Mean 588

11.3.2 The Statistics and Semantics 593

11.4 Benchmarking 595

11.4.1 Clock Rate, MIPS, and FLOPS 596

11.4.2 Synthetic Benchmarks: Whetstone, Linpack, and Dhrystone 598

xiv Contents

11.4.3	Standard Performance Evaluation Corporation Benchmarks	599
11.4.4	Transaction Processing Performance Council Benchmarks	603
11.4.5	System Simulation	609
11.5	CPU Performance Optimization	611
11.5.1	Branch Optimization	611
11.5.2	Use of Good Algorithms and Simple Code	614
11.6	Disk Performance	617
11.6.1	Understanding the Problem	618
11.6.2	Physical Considerations	620
11.6.3	Logical Considerations	620
	Chapter Summary	625
	Further Reading	626
	References	628
	Review of Essential Terms and Concepts	629
	Exercises	629

**CHAPTER
12****Network Organization and Architecture****635**

12.1	Introduction	635
12.2	Early Business Computer Networks	635
12.3	Early Academic and Scientific Networks: The Roots and Architecture of the Internet	636
12.4	Network Protocols I: ISO/OSI Protocol Unification	640
12.4.1	A Parable	641
12.4.2	The OSI Reference Model	642
12.5	Network Protocols II: TCP/IP Network Architecture	646
12.5.1	The IP Layer for Version 4	646
12.5.2	The Trouble with IP Version 4	650
12.5.3	Transmission Control Protocol	654
12.5.4	The TCP Protocol at Work	655
12.5.5	IP Version 6	659
12.6	Network Organization	666
12.6.1	Physical Transmission Media	666
12.6.2	Interface Cards	674
12.6.3	Repeaters	674
12.6.4	Hubs	675
12.6.5	Switches	675
12.6.6	Bridges and Gateways	676
12.6.7	Routers and Routing	678

12.7	High-Capacity Digital Links	687
12.7.1	The Digital Hierarchy	687
12.7.2	ISDN	692
12.7.3	Asynchronous Transfer Mode	695
12.8	A Look at the Internet	696
12.8.1	Ramping on to the Internet	697
12.8.2	Ramping up the Internet	704
	Chapter Summary	705
	Further Reading	705
	References	707
	Review of Essential Terms and Concepts	707
	Exercises	709

CHAPTER
13
Selected Storage Systems and Interfaces
713

13.1	Introduction	713
13.2	SCSI Architecture	714
13.2.1	“Classic” Parallel SCSI	715
13.2.2	The SCSI Architecture Model-3	719
13.3	Internet SCSI	726
13.4	Storage Area Networks	729
13.5	Other I/O Connections	729
13.5.1	Parallel Buses: XT to ATA	730
13.5.2	Serial ATA and Serial Attached SCSI	731
13.5.3	Peripheral Component Interconnect	732
13.5.4	A Serial Interface: USB	733
13.5.5	High Performance Peripheral Interface: HiPPI	733
13.6	Cloud Storage	734
	Chapter Summary	734
	Further Reading	735
	References	736
	Review of Essential Terms and Concepts	736
	Exercises	737

APPENDIX
A
Data Structures and the Computer
739

A.1	Introduction	739
A.2	Fundamental Structures	739

xvi Contents

- A.2.1 Arrays 739
- A.2.2 Queues and Linked Lists 741
- A.2.3 Stacks 742
- A.3 Trees 745**
- A.4 Network Graphs 751**
- Summary 754
- Further Reading 754
- References 754
- Exercises 755

Glossary	759
-----------------	------------

Answers and Hints for Selected Exercises	801
---	------------

Index	817
--------------	------------