

## DM74LS47

### BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

#### General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250  $\mu$ A. Auxiliary inputs provided blanking, lamp test and cascable zero-suppression functions.

#### Features

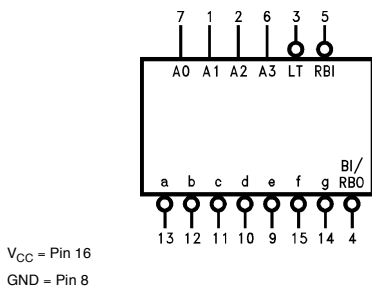
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

#### Ordering Code:

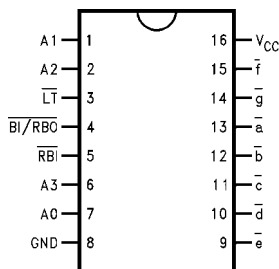
Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
RBI	Ripple Blanking Input (Active LOW)
LT	Lamp Test Input (Active LOW)
BI/RBO	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a–g	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

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## Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A3	A2	A1	A0	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

**Note 2:**  $\overline{\text{BI/RBO}}$  is wire-AND logic serving as blanking input ( $\overline{\text{BI}}$ ) and/or ripple-blanking output ( $\overline{\text{RBO}}$ ). The blanking out ( $\overline{\text{BI}}$ ) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ( $\overline{\text{RBI}}$ ) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

**Note 3:** When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

**Note 4:** When ripple-blanking input ( $\overline{\text{RBI}}$ ) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ( $\overline{\text{RBO}}$ ) goes to a LOW level (response condition).

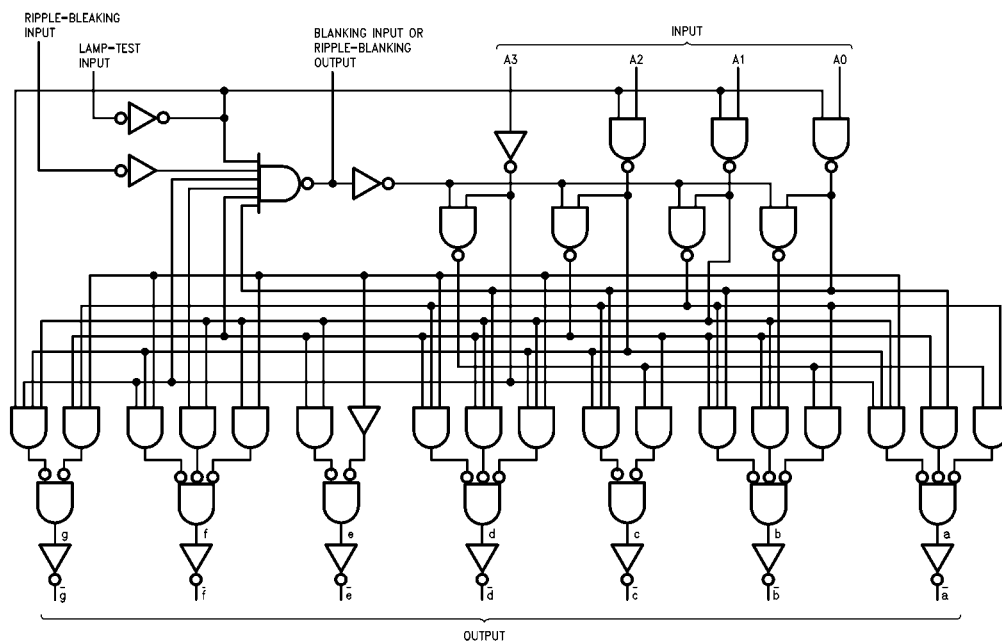
**Note 5:** When the blanking input/ripple-blanking output ( $\overline{\text{BI/RBO}}$ ) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

## Functional Description

The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the  $\overline{\text{RBI}}$  blanks the display and causes a multi-digit display. For example, by grounding the  $\overline{\text{RBI}}$  of the highest order decoder and connecting its  $\overline{\text{BI/RBO}}$  to  $\overline{\text{RBI}}$  of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding  $\overline{\text{RBI}}$  of the lowest order decoder and connecting its  $\overline{\text{BI/RBO}}$  to  $\overline{\text{RBI}}$  of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving  $\overline{\text{RBI}}$  of a

intermediate decoder from an OR gate whose inputs are  $\overline{\text{BI/RBO}}$  of the next highest and lowest order decoders.  $\overline{\text{BI/RBO}}$  also serves as an unconditional blanking input. The internal NAND gate that generates the  $\overline{\text{RBO}}$  signal has a resistive pull-up, as opposed to a totem pole, and thus  $\overline{\text{BI/RBO}}$  can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to  $\overline{\text{BI/RBO}}$  turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to  $\overline{\text{LT}}$  turns on all segment outputs, provided that  $\overline{\text{BI/RBO}}$  is not forced LOW.

## Logic Diagram



## Numerical Designations—Resultant Displays

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	c	3	4	5	t	